

CLAIMS:

1. A method of forming silicon nitride on a silicon-oxide-comprising material, comprising:

exposing the silicon-oxide-comprising material to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into an upper portion of the material; the silicon-oxide-comprising material being maintained at a temperature of less than or equal to 200°C during the exposing;

thermally annealing the nitrogen within the material to bond at least some of the nitrogen to silicon proximate the nitrogen; and

after the annealing, chemical vapor depositing silicon nitride on the nitrogen-containing upper portion of the material.

2. The method of claim 1 wherein the silicon-oxide-comprising material comprises silicon dioxide.

3. The method of claim 1 wherein the silicon-oxide-comprising material consists essentially of silicon dioxide.

4. The method of claim 1 wherein the silicon-oxide-comprising material is at least 10Å thick, and wherein substantially all of the nitrogen is within the top 5Å of the silicon-oxide-comprising material.

1 5. The method of claim 1 wherein the silicon-oxide-comprising
2 material is less than or equal to about 5Å thick, and wherein the
3 chemical vapor deposited silicon is at least about 10Å thick.

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5 6. The method of claim 1 wherein the silicon-oxide-comprising
6 layer is less than or equal to about 10Å thick, and wherein the chemical
7 vapor deposited silicon is at least about 30Å thick.

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9 7. The method of claim 1 wherein the silicon-oxide-comprising
10 material is less than or equal to about 10Å thick, wherein the thermally
11 annealed nitrogen is only within the top half of the silicon-oxide-
12 comprising material, and wherein the chemical vapor deposited silicon is
13 at least about 30Å thick.

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15 8. The method of claim 1 wherein the silicon-oxide-comprising
16 material is maintained at a temperature of from 50°C to 200°C during
17 the exposing.

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19 9. The method of claim 1 wherein the plasma is maintained
20 with a power of from about 500 watts to about 5000 watts during the
21 exposing.

1 10. The method of claim 1 wherein the plasma is maintained
2 with a power of from about 500 watts to about 3000 watts during the
3 exposing.

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5 11. The method of claim 1 wherein the exposing occurs within
6 a reactor, and wherein a pressure within the reactor is less than or
7 equal to about 3 Torr during the exposing.

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9 12. The method of claim 1 wherein the exposing occurs within
10 a reactor, and wherein a pressure within the reactor is from about
11 5 mTorr to about 10 mTorr during the exposing.

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13 13. The method of claim 1 wherein the exposing occurs for a
14 time of less than or equal to about 1 minute.

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16 14. The method of claim 1 wherein the exposing occurs for a
17 time of from about 3 seconds to about 1 minute.

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19 15. The method of claim 1 wherein the exposing occurs for a
20 time of from about 10 seconds to about 15 seconds.

1 16. The method of claim 1 wherein the annealing comprises
2 rapid thermal processing at a ramp rate of at least about 50°C/sec to
3 a temperature of less than 1000°C, with such temperature being
4 maintained for at least about 30 seconds.

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6 17. The method of claim 1 wherein the annealing comprises
7 thermal processing at temperature of less than 1100°C for a time of at
8 least 3 seconds.
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1 18. A method of forming a transistor device, comprising:
2 forming a silicon-oxide-comprising layer over a substrate;
3 exposing the silicon-oxide-comprising layer to activated nitrogen
4 species from a nitrogen-containing plasma to introduce nitrogen into an
5 upper portion of the layer;
6 thermally annealing the nitrogen within the layer to bond at least
7 some of the nitrogen to silicon proximate the nitrogen;
8 after the annealing, chemical vapor depositing silicon nitride on the
9 nitrogen-containing upper portion of the layer;
10 forming at least one conductive gate layer over the silicon nitride,
11 the gate layer defining a channel region in the substrate beneath the
12 silicon nitride; and
13 forming a pair of source/drain regions proximate the gate layer and
14 gatedly connected to one another through the channel region.

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16 19. The method of claim 18 wherein the silicon-oxide-comprising
17 layer comprises silicon dioxide.

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19 20. The method of claim 18 wherein the silicon-oxide-comprising
20 layer consists essentially of silicon dioxide.
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1 21. The method of claim 18 wherein the silicon-oxide-comprising
2 layer is at least 10Å thick, and wherein substantially all of the nitrogen
3 is within the top 5Å of the silicon-oxide-comprising layer.
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5 22. The method of claim 18 wherein the silicon-oxide-comprising
6 layer is less than or equal to about 5Å thick, and wherein the chemical
7 vapor deposited silicon is at least about 10Å thick.
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9 23. The method of claim 18 wherein the silicon-oxide-comprising
10 layer is less than or equal to about 10Å thick, and wherein the chemical
11 vapor deposited silicon is at least about 30Å thick.
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13 24. The method of claim 18 wherein the silicon-oxide-comprising
14 layer is less than or equal to about 10Å thick, wherein the thermally
15 annealed nitrogen is only within the top half of the silicon-oxide-
16 comprising layer, and wherein the chemical vapor deposited silicon is at
17 least about 30Å thick.
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19 25. The method of claim 18 wherein the substrate comprises a
20 semiconductive material, and wherein the source/drain regions are formed
21 as diffusion regions in the semiconductive material of the substrate.
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1 26. The method of claim 18 wherein the silicon-oxide-comprising
2 material consists essentially of silicon dioxide.

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4 27. The method of claim 18 wherein the silicon-oxide-comprising
5 material is maintained at a temperature of from 50°C to 200°C during
6 the exposing.

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8 28. The method of claim 18 wherein the plasma is maintained
9 with a power of from about 500 watts to about 5000 watts during the
10 exposing.

11
12 29. The method of claim 18 wherein the plasma is maintained
13 with a power of from about 500 watts to about 3000 watts during the
14 exposing.

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16 30. The method of claim 18 wherein the exposing occurs for a
17 time of less than or equal to about 1 minute.

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19 31. The method of claim 18 wherein the exposing occurs for a
20 time of from about 3 seconds to about 1 minute.

1 32. The method of claim 18 wherein the exposing occurs for a
2 time of from about 10 seconds to about 15 seconds.

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4 33. The method of claim 18 wherein the annealing comprises
5 rapid thermal processing at a ramp rate of at least about 50°C/sec to
6 a temperature of less than 1000°C, with such temperature being
7 maintained for at least about 30 seconds.

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9 34. The method of claim 18 wherein the annealing comprises
10 thermal processing at temperature of less than 1100°C for a time of at
11 least 3 seconds.

1 35. A transistor device, comprising:
2 a silicon-oxide-comprising material over a substrate, the silicon-
3 oxide-comprising material having a thickness of less than or equal to
4 about 10Å;
5 a silicon-nitride-comprising material on the silicon-oxide-comprising
6 layer, the silicon-nitride-comprising material having a thickness of at least
7 30Å, the silicon-nitride-comprising material being different than the
8 silicon-oxide-comprising material;
9 at least one conductive gate layer on the silicon-nitride-comprising
10 material, the gate layer defining a channel region in the substrate
11 beneath the silicon-oxide-comprising material; and
12 a pair of source/drain regions proximate the gate layer and gatedly
13 connected to one another through the channel region.

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15 36. The device of claim 35 wherein the silicon-oxide-comprising
16 material does not comprise nitrogen.

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18 37. The device of claim 35 wherein the silicon-nitride-comprising
19 material has a thickness of at least about 40Å.

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21 38. The device of claim 35 wherein the silicon-oxide-comprising
22 material has a thickness of 5Å or less.
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1 39. The device of claim 35 wherein the silicon-nitride-comprising
2 material has a thickness of at least about 40Å, and wherein the silicon-
3 oxide-comprising material has a thickness of 5Å or less.

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5 40. The device of claim 35 wherein the substrate comprises
6 monocrystalline silicon, and wherein the source/drain regions are
7 conductively doped diffusion regions within the substrate.